TEXAS INSTRUMENTS

# TPS54980EVM-022 9-Amp, SWIFT™ Regulator Evaluation Module

# User's Guide

September 2003

PMP Systems Power

SLVU090

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# Contents


**1 Introduction . . . . . 1-1**
1.1 Background . . . . . 1-2
1.2 Performance Specification Summary . . . . . 1-3
1.3 Modifications . . . . . 1-4
1.3.1 Changing Output Voltage . . . . . 1-4
1.3.2 Switching Frequency . . . . . 1-4
1.3.3 Power Sequencing . . . . . 1-5

**2 Test Setup and Results . . . . . 2-1**
2.1 Input/Output Connections . . . . . 2-2
2.2 Efficiency . . . . . 2-3
2.3 Power Dissipation . . . . . 2-4
2.4 Output Voltage Regulation . . . . . 2-5
2.5 Load Transients . . . . . 2-6
2.6 Loop Characteristics . . . . . 2-6
2.7 Output Voltage Ripple . . . . . 2-7
2.8 Input Voltage Ripple . . . . . 2-8
2.9 Power Up and Down . . . . . 2-9

**3 Board Layout . . . . . 3-1**
3.1 Layout . . . . . 3-2

**4 Schematic and Bill of Materials . . . . . 4-1**
4.1 Schematic . . . . . 4-2
4.2 Bill of Materials . . . . . 4-3

# Figures


1−1 Frequency Trimming Resistor Selection Graph . . . . . 1-5
2−1 Connection Diagram . . . . . 2-2
2−2 Measured Efficiency, TPS54980 . . . . . 2-3
2−3 Measured Circuit Losses . . . . . 2-4
2−4 Load Regulation . . . . . 2-5
2−5 Line Regulation . . . . . 2-5
2−6 Load Transient Response, TPS54980 . . . . . 2-6
2−7 Measured Loop Response, TPS54980, $V_I$ = 3 V . . . . . 2-6
2−8 Measured Loop Response, TPS54980, $V_I$ = 4 V . . . . . 2-7
2−9 Measured Output Voltage Ripple, TPS54980 . . . . . 2-7
2−10 Input Voltage Ripple, TPS54980 . . . . . 2-8
2−11 Power Up with Tracking . . . . . 2-9
2−12 Power Down With Tracking . . . . . 2-10
2−13 Power Up With Ratiometric Sequencing . . . . . 2-10
2−14 Power Down With Ratiometric Sequencing . . . . . 2-11
2−15 Power Up With Core Voltage Rising First . . . . . 2-11
2−16 Power Up With Core Voltage Falling Second . . . . . 2-12
3−1 Top-Side Layout . . . . . 3-2
3−2 Internal Layer 2 . . . . . 3-3
3−3 Internal Layer 3 . . . . . 3-3
3−4 Bottom Side Layout (looking from top side) . . . . . 3-4
3−5 Top Side Assembly . . . . . 3-4
4−1 TPS54980EVM-022 Schematic . . . . . 4-2


# Tables


1−1 Input Voltage and Output Current Summary . . . . . 1-2
1−2 TPS54980EVM-022 Performance Specification Summary . . . . . 1-3
1−3 Output Voltage Programming . . . . . 1-4
4−1 TPS54980EVM-022 Bill of Materials . . . . . 4-3

# Read This First

## About This Manual

This user's guide describes the characteristics, operation, and the use of the TPS54980EVM-022 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

## How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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# Chapter 1

# Introduction

This chapter contains background information for the TPS54980 as well as support documentation for the TPS54980EVM-022 evaluation module (HPA022). The TPS54980EVM-022 performance specifications are given, as well as modifications.

**Topic** **Page**


| | | |
|---|---|---|
| 1.1 | Background | 1-2 |
| 1.2 | Performance Specification Summary | 1-3 |
| 1.3 | Modifications | 1-4 |

## 1.1 Background

The TPS54980 tracking dc/dc converter is designed to provide accurate power sequencing in applications where two or more voltages are required for a load. These types of applications include core and I/O power supplies for microprosessors, DSPs, and FPGAs. Typically, some specific relation between the core and I/O supply voltages has to be provided during the power up and power down sequences. The TPS54980 tracking dc/dc converter is capable of direct tracking, ratiometric tracking, and voltage sequencing with a second power source.

The TPS54980EVM−022 is a two-channel EVM demonstrating the flexibility inherent in the TPS54980 design for tracking and sequencing core and I/O voltages. The TPS54980 is used to generate the core voltage and is nominally set at 1.8 V. The nominal 3.3-V I/O voltage is provided by a TPS2013 distribution switch. Rated input voltage and output current range are listed in Table 1−1.

*Table 1−1. Input Voltage and Output Current Summary*

| EVM | Input Voltage Range | Output Current Range |
|---|---|---|
| TPS54980EVM−022 | 3.0 V to 4.0 V | Core, −9 A to 9 A |
| | | I/O, 0 to 1.5 A |

This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54980 regulator. The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.65-µH output inductor.

The MOSFETs of the TPS54980 are incorporated inside the TPS54980 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs provides the TPS54980 high efficiency and helps to keep the junction temperature low at high output currents.The compensation components are provided external to the IC and allow for an adjustable output voltage and a customizable loop response.

The TPS54980 device uses the TRACKIN pin to access the tracking and sequencing capabilities. An internal multiplexer circuit compares the voltage at this pin with the internal reference voltage and uses the lesser of the two as the reference for the output voltage regulation. When the output of another power supply or distribution switch is connected to the TRACKIN pin of the TPS54980, the output of the TPS54980 tracks the output of this other channel during power up or power down, until the voltage at the TRACKIN pin becomes higher than the internal reference voltage. By applying the other power supply output to the TRACKIN pin through an appropriate resistor divider network, any required power up and power down relation between the two output voltages of the regulators can be set by changing the ratio of the divider network.

## 1.2 Performance Specification Summary

A summary of the TPS54980EVM−022 performance specifications is provided in Table 1−2. Specifications are given for an input voltage of 3.3 V and an output voltage of 1.8 V unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted. The data presented in Table 1−2 was compiled with no load on the I/O output. The maximum input voltage for the TPS54980 is 4 V.

*Table 1−2. TPS54980EVM-022 Performance Specification Summary*

| Parameters | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input voltage range | | | 3.0 | 3.3 | 4.0 | V |
| Output voltage set point | | | | 1.8 | | V |
| Output current range | | $V_I$ = 3 to 5.5 V | −9 | | 9 | A |
| Line regulation | | $I_O$ = 0 A to 3 A, $V_I$ = 3 V to 5.5 V | | ±0.1% | | |
| Load regulation | | $V_I$ = 3.3 V, $I_O$ = 0 to 3 A | | ±0.2% | | |
| Load transient response | Voltage change | $I_O$ = 2.25 A to 6.75 A | | −50 | | $mV_{PK}$ |
| | Recovery time | | | 400 | | µs |
| | Voltage change | $I_O$ = 6.75 A to 2.25 A | | 50 | | $mV_{PK}$ |
| | Recovery time | | | 400 | | µs |
| Loop bandwidth | | $V_I$ = 3 V | | 63 | | kHz |
| Phase margin | | $V_I$ = 3 V | | 56 | | ° |
| Loop bandwidth | | $V_I$ = 4 V | | 75 | | kHz |
| Phase margin | | $V_I$ = 4 V | | 49 | | ° |
| Input ripple voltage | | | | 50 | 200 | $mV_{PP}$ |
| Output ripple voltage | | | | 6 | 10 | $mV_{PP}$ |
| Output rise time | | | | N/A | | ms |
| Operating frequency | | | 280 | 700 | 700 | kHz |
| Max efficiency | | $V_I$ = 3.3 V, $V_O$ = 1.8 V, $I_O$ = 1.0 A | | 89% | | |

## 1.3 Modifications

The TPS54980EVM-022 is designed to demonstrate the small size that can be attained when designing with the TPS54980, however many of the features, which allow for extensive modifications, have been omitted from this EVM.

### 1.3.1 Changing Output Voltage

By changing the value of $R_2$, the output voltage can be set to a value in the range of 0.9 V to 2.5 V. The value of $R_2$ for a specific output voltage can be calculated by using Equation 1−1. Table 1−3 lists the values for $R_2$ for some common output voltages.

*Equation 1−1.*

$$R_2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V}$$

*Table 1−3. Output Voltage Programming*

| Output Voltage (V) | $R_2$ Value (kΩ) |
|---|---|
| 0.9 | 1000 |
| 1.2 | 28.7 |
| 1.5 | 14.7 |
| 1.8 | 9.76 |
| 2.5 | 5.49 |

The minimum output voltage is limited by the minimum controllable on-time of the device, 200 ns, and is dependent upon the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 1−2:

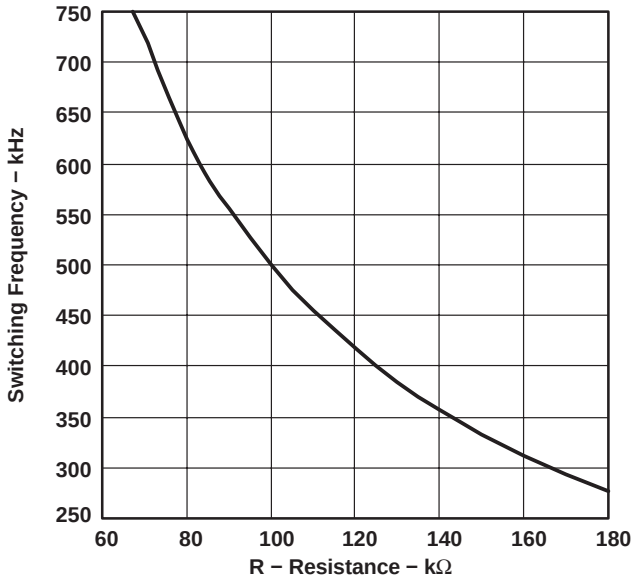
*Equation 1−2.*

$$V_{OUTMIN} = 200\ nsec \times f_s \times V_{INMAX}$$

### 1.3.2 Switching Frequency

Switching frequency can be trimmed to any value between 280 kHz and 700 kHz by changing the value of R4. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased. A plot of the value of RT versus the switching frequency is shown in Figure 1−1.

*Figure 1−1. Frequency Trimming Resistor Selection Graph*




An onboard electrolytic input capacitor may be added at C1.

### 1.3.3 Power Sequencing

By selecting different R6−R7 resistor divider ratios, different power sequencing scenarios can be set. The Equations 1−3, 1−4, and 1−5 show how to select the different ways of power sequencing.

*Equation 1−3.*

$$\frac{R6}{R7} = \frac{R1}{R2}$$ − Core voltage tracks I/O voltage

*Equation 1−4.*

$$\frac{R6}{R7} = \frac{\left(V_{I/O} - 0.891\right)}{0.891}$$ − Ratiometric relation between core and I/O voltage

*Equation 1−5.*

$$\frac{R6}{R7} < \frac{R1}{R2}$$ − Core voltage rises first at power up and falls second at power down

Chapter 2

# Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54980EVM-022 evaluation module. The chapter also includes test results typical for the TPS54980EVM-022 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

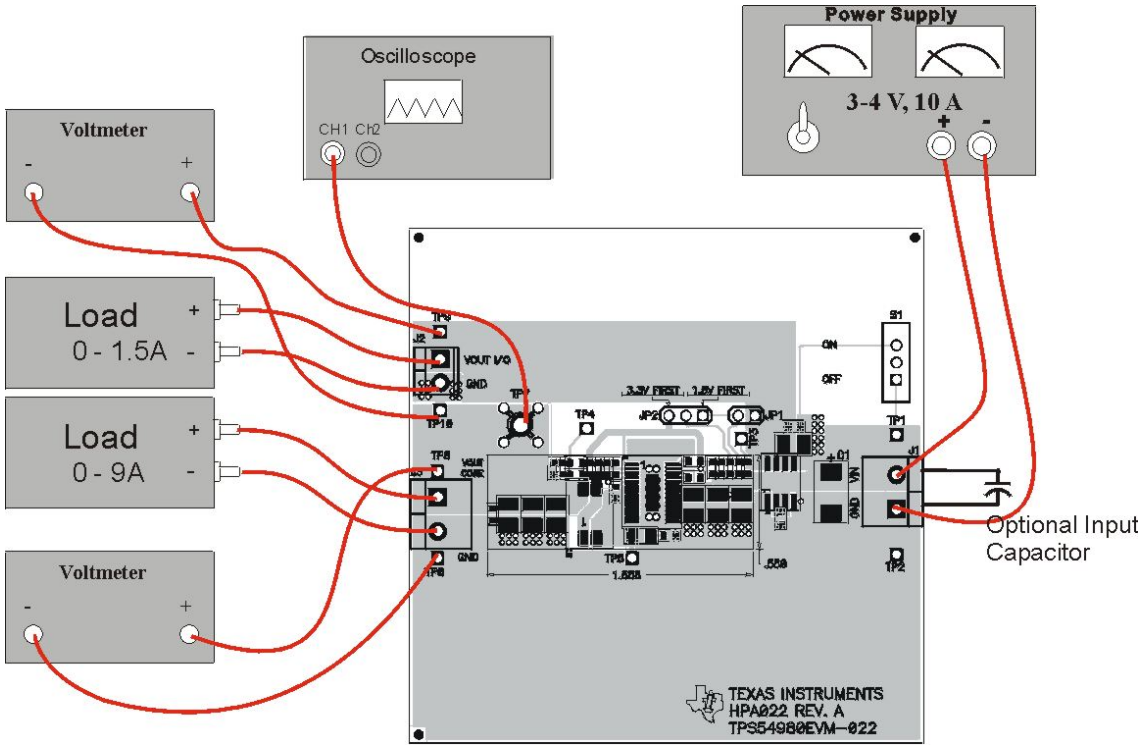
**Topic** **Page**


| | | |
|---|---|---|
| 2.1 | Input/Output Connections | 2-2 |
| 2.2 | Efficiency | 2-3 |
| 2.3 | Power Dissipation | 2-4 |
| 2.4 | Output Voltage Regulation | 2-5 |
| 2.5 | Load Transients | 2-6 |
| 2.6 | Loop Characteristics | 2-6 |
| 2.7 | Output Voltage Ripple | 2-7 |
| 2.8 | Input Voltage Ripple | 2-8 |
| 2.9 | Power Up and Down | 2-9 |

## 2.1 Input/Output Connections

The TPS54980EVM−022 has the following three input/output connectors: VIN J1, VOUT I/O J2, and VOUT CORE J3. A diagram showing the connection points is shown in Figure 2−1. A power supply capable of supplying 8 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J2 through a pair of 16 AWG wires. The maximum load current capability should be 9 A. Wire lengths should be minimized to reduce losses in the wires. Test point TP7 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54980 is intended to be used as a point of load regulator. In typical applications it is usually located close to the input voltage source. When using the TPS54980EVM−022 with an external power supply as the source for VIN, an additional bulk capacitor may be required, depending upon the output impedance of the source and length of the hook-up wires. The test results presented were obtained using an additional 470-µF, 16-V input capacitor. Alternately, C1 may be populated with an input filter capacitor. Connection is shown for no load on the I/O voltage output. The I/O voltage may supply up to 1.5 A into an external load.

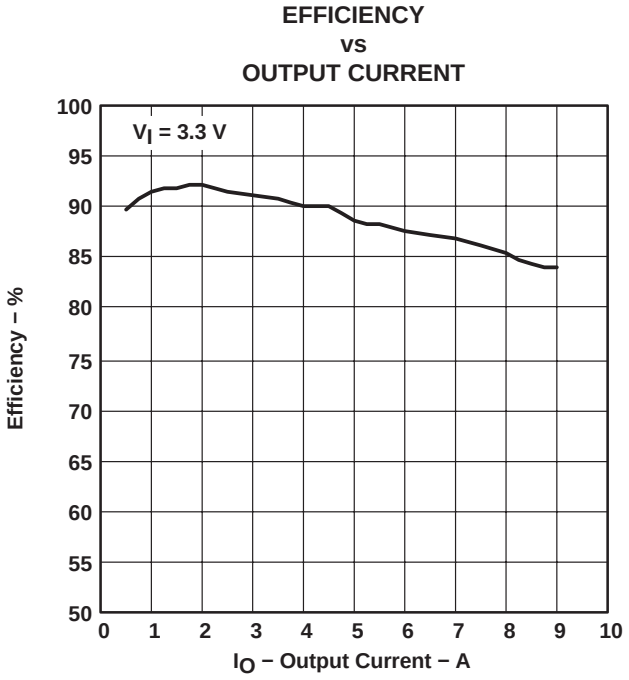
*Figure 2−1. Connection Diagram*



## 2.2 Efficiency

The TPS54980EVM−022 efficiency peaks at a load current of about 1 A to 2 A and then decreases as the load current increases towards full load. Figure 2−2 shows the efficiency of the TPS54980 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the MOSFETs. Efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

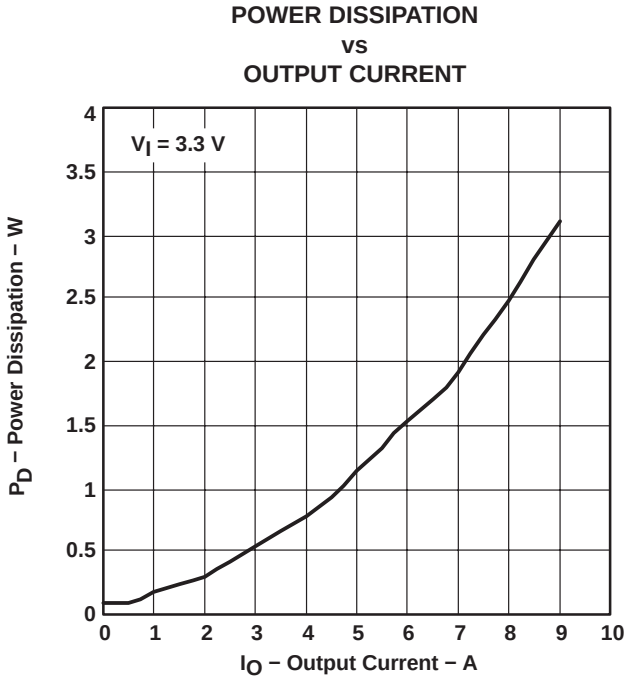
*Figure 2−2. Measured Efficiency, TPS54980*



## 2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with well designed board layout, allows the TPS54980EVM-022 EVM to output full rated load current while maintaining safe junction temperatures. With a 3.3-V input source and a 9-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C. The total circuit losses at 25°C are shown in Figure 2−3. Power dissipaton is shown for an input voltage of 3.3 V. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

*Figure 2−3. Measured Circuit Losses*



## 2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54980EVM−022 is shown in Figure 2−4, while the output voltage line regulation is shown in Figure 2−5. Measurements are shown for an ambient temperature of 25°C.

*Figure 2−4. Load Regulation*

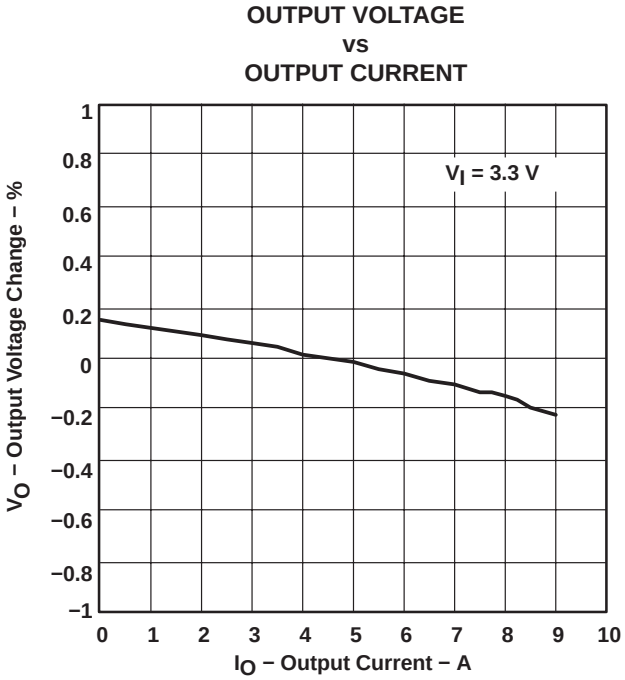
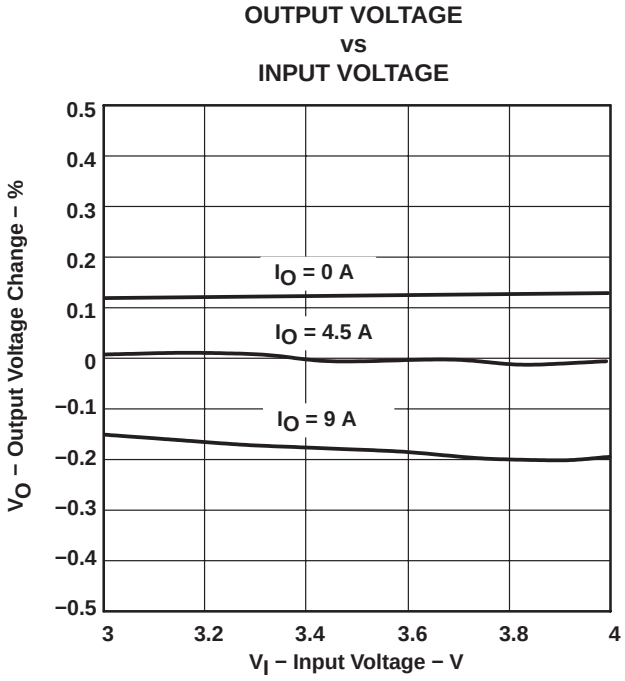


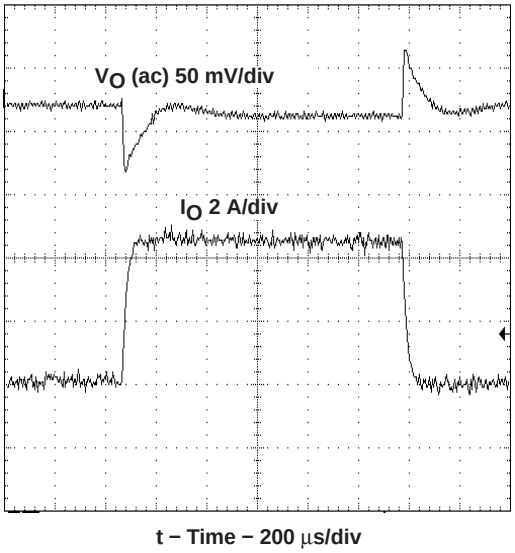

*Figure 2−5. Line Regulation*



## 2.5 Load Transients

The TPS54980EVM−022 response to load transients is shown in Figure 2−6. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

*Figure 2−6. Load Transient Response, TPS54980*




## 2.6 Loop Characteristics

The TPS54980EVM−022 loop response characteristics are shown in Figure 2−7 and Figure 2−8. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

*Figure 2−7. Measured Loop Response, TPS54980, $V_I$ = 3V*

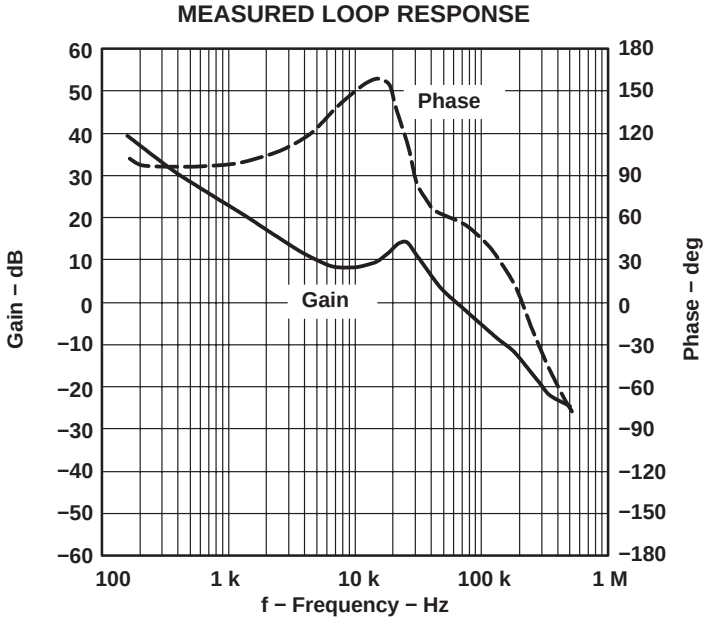
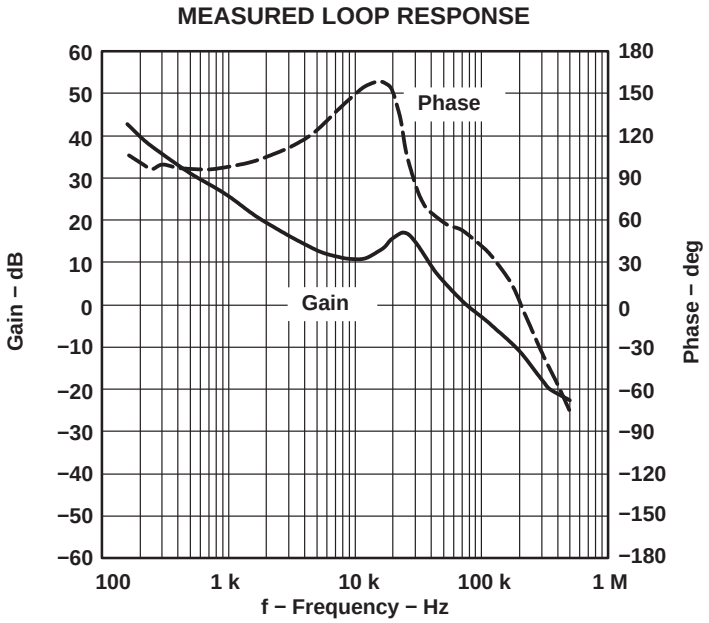


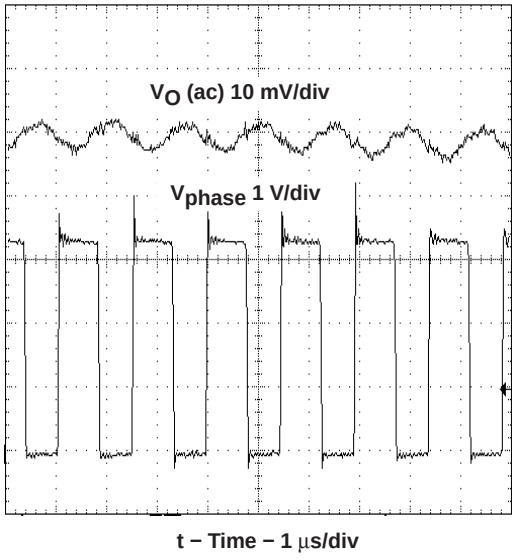
*Figure 2−8. Measured Loop Response, TPS54980, $V_I$ = 4*




## 2.7 Output Voltage Ripple

The TPS54980EVM−022 output voltage ripple is shown in Figure 2−9. The input voltage is 3.3 V for the TPS54980. Output current is the rated full load of 9 A. Voltage is measured directly across output capacitors.

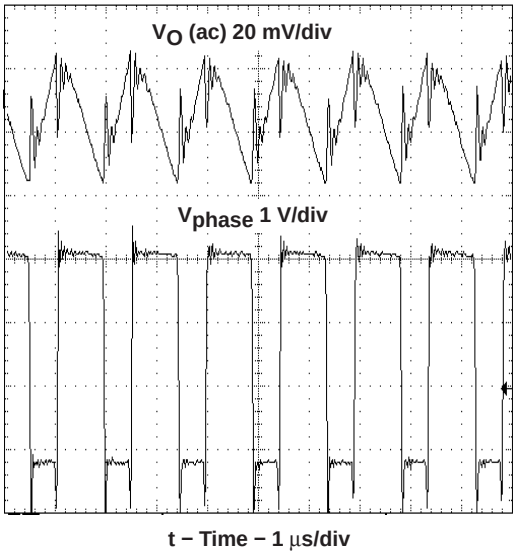
*Figure 2−9. Measured Output Voltage Ripple, TPS54980*



## 2.8 Input Voltage Ripple

The TPS54980EVM−022 output voltage ripple is shown in Figure 2−10. The input voltage is 3.3 V for the TPS54980. Output current for each device is the rated full load of 9 A.

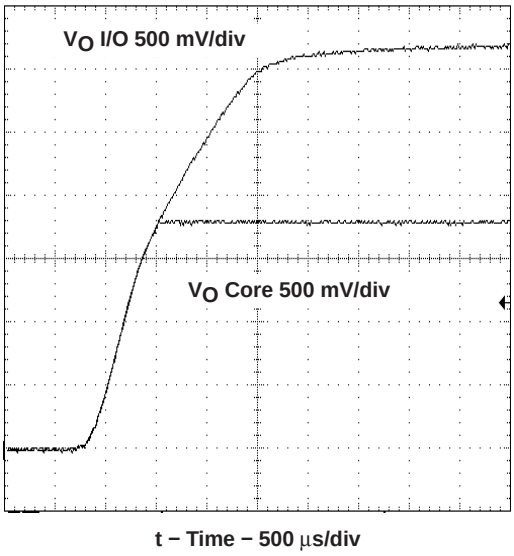
*Figure 2−10. Input Voltage Ripple, TPS54980*



## 2.9 Power Up and Down

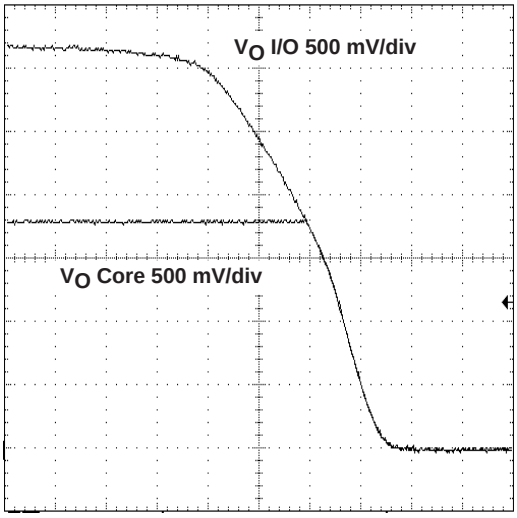
The TPS54980 regulator provides different modes for power up and power down sequencing of the core and I/O voltages. By selecting different ratios for the resistor divider R6/R7 (see Figure 4−1), the slope of the core voltage during power up and down can be set equal to, higher than, or lower than the slope of the I/O voltage. If the resistors R6 = R1 and R7 = R2, then the core voltage tracks the I/O voltage. The start up voltage waveform of the TPS54980EVM-022 for this condition is shown in Figure 2−11. The waveform shows that the core voltage regulator tracks the output of the I/O regulator until the core regulator reaches its nominal 1.8-V level. After that, the core regulator starts to regulate its output at the preset 1.8-V level. The I/O regulator continues its ramp up until the voltage reaches the nominal 3.3-V level. The output voltage waveforms during power up do not depend on load currents. The output voltage waveforms are powered up by asserting the ENABLE signal while the input voltage is already applied.

*Figure 2−11. Power Up with Tracking*




The power down waveform is shown in Figure 2−12. During power down, the output voltage fall time is defined by the output capacitance and load resistance. In this case the I/O output load resistance has been set to 20 Ω and the core output load resistance set to 1 Ω. With the I/O output voltage falling with a slew rate of about 1.25 V/ms, there is essentially no difference between the core voltage and I/O voltage.

*Figure 2−12. Power Down With Tracking*




The TPS54980EVM-022 EVM provides the ability to change the slew rate of the output voltage of the core regulator by using jumper JP2 (see schematic in Figure 4−1). If jumper JP2 is set so that R8 is connected in parallel to R7, ratiometric power sequencing is implemented. For ratiometric sequencing, the following condition must to be met: if R6 = 10 kΩ then R8 II R7 = (R7 × 0.891)/($V_{I/O}$ − 0.891). In this case, the I/O and core voltages reach their nominal values at the same time. The waveforms for ratiometric power up and down are shown in Figure 2−13 and Figure 2−14.

*Figure 2−13. Power Up With Ratiometric Sequencing*

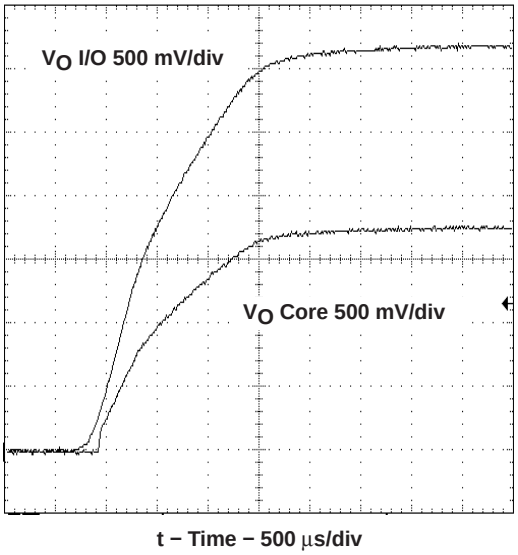
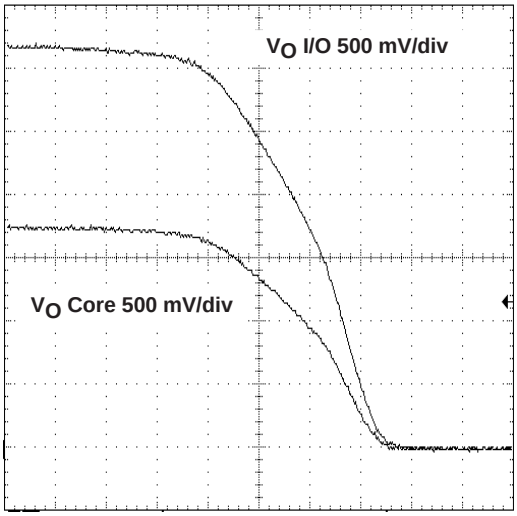


*Figure 2−14. Power Down With Ratiometric Sequencing*




If jumper JP2 is set so that R8 is connected in parallel to R6, the core voltage rises first during power up and falls second during power down. The waveforms with this type of sequencing are shown in Figure 2−15 and Figure 2−16.

*Figure 2−15. Power Up With Core Voltage Rising First*

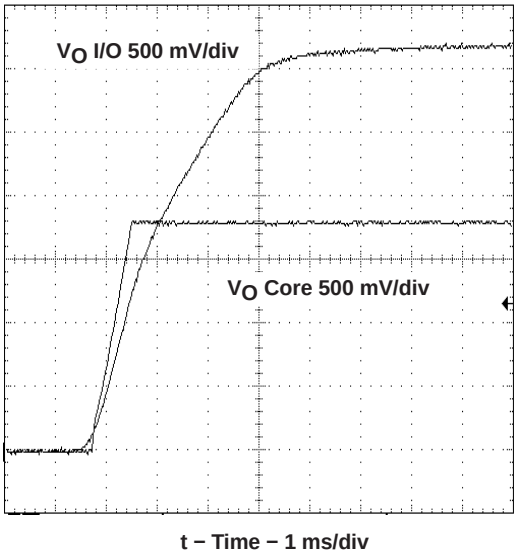
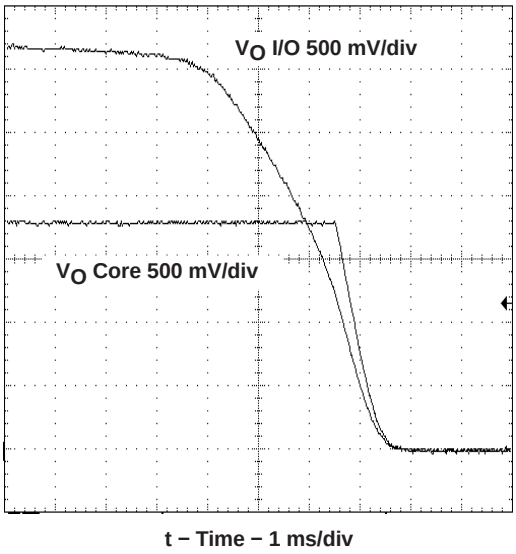


*Figure 2−16. Power Up With Core Voltage Falling Second*



# Chapter 3

# Board Layout

This chapter provides a description of the TPS54980EVM-022 board layout and layer illustrations.

**Topic** **Page**

**3.1 Layout ..... 3-2**

## 3.1 Layout

The board layout for the TPS54980EVM−022 is shown in Figure 3−1 through Figure 3−6. The topside layer of the TPS54980EVM−022 is laid out in a manner typical of a user application. The top and bottom layers are 1.5-oz. copper, while the two internal ground plane layers are 1-oz. copper.

The top layer contains the main power traces for $V_I$, $V_O$, and $V_{phase}$. Also on the top layer are connections for the remaining pins of the TPS54980 and a large area filled with ground. The bottom layer contains ground and some signal routing. The top and bottom ground traces are connected with multiple vias placed around the board including 12 directly under the TPS54980 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C5, C9, and C19), bias decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

*Figure 3−1. Top-Side Layout*

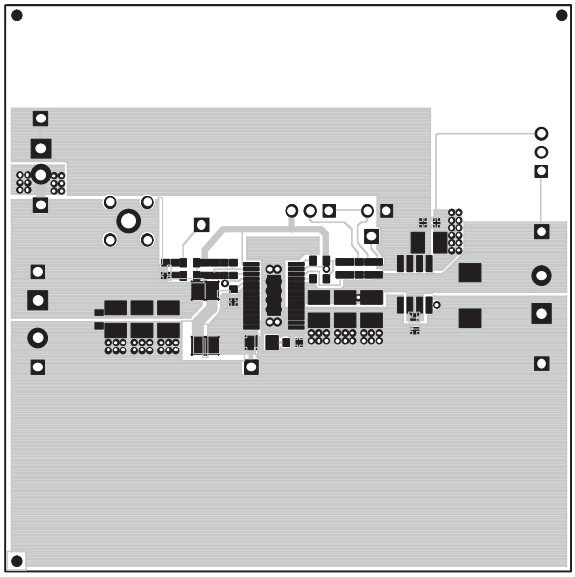


*Figure 3−2. Internal Layer 2*

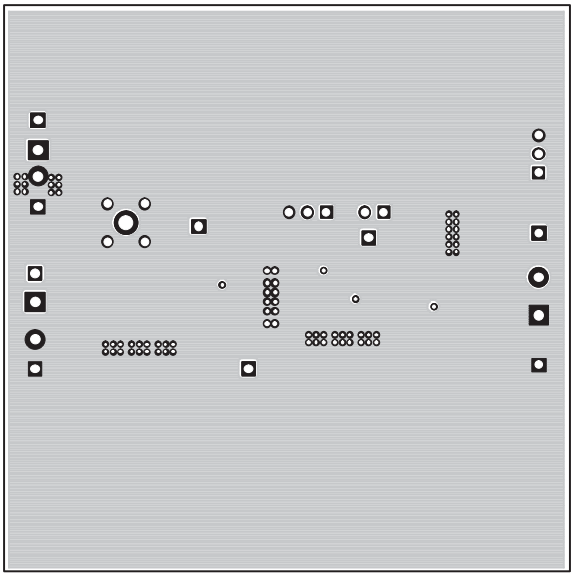


*Figure 3−3. Internal Layer 3*

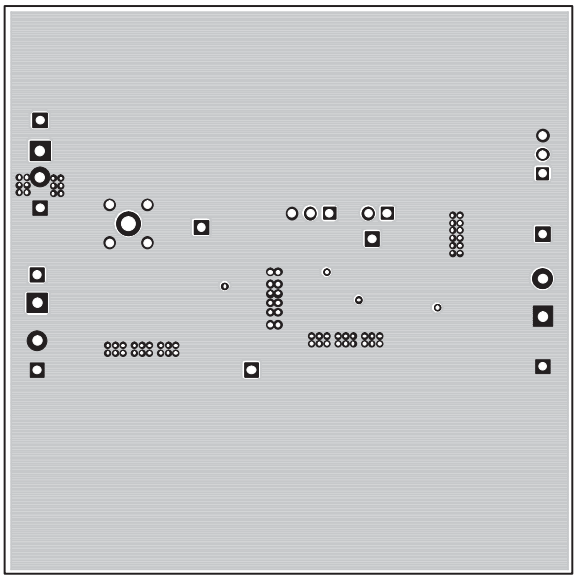


*Figure 3−4. Bottom Side Layout (looking from top side)*

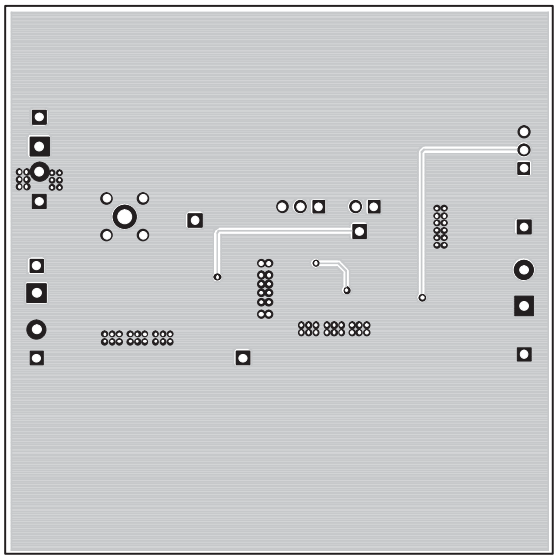
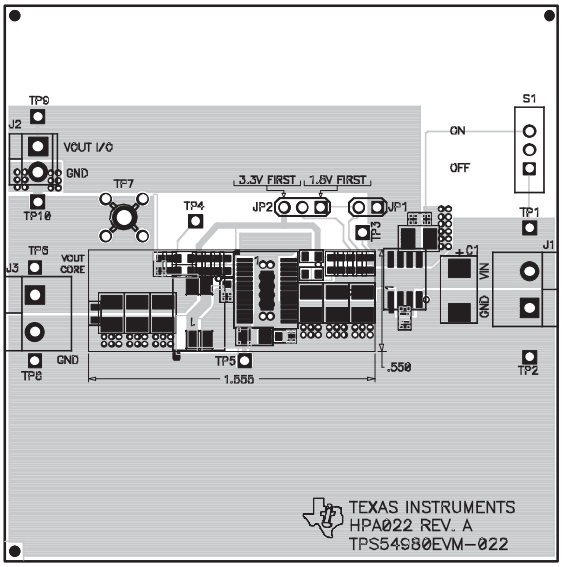


*Figure 3−5. Top Side Assembly*



Chapter 4

# Schematic and Bill of Materials

The TPS54980EVM-022 schematic and bill of materials are presented in this chapter.

**Topic** **Page**

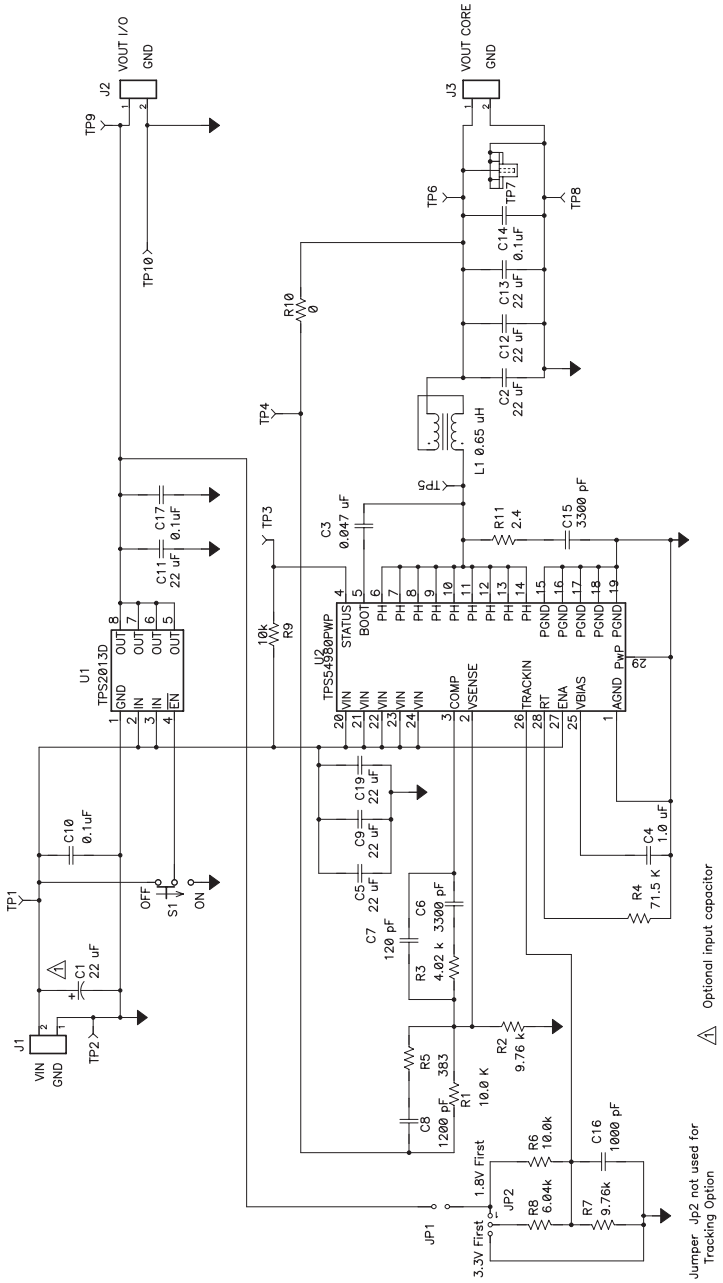

**4.1 Schematic** . . . . . **4-2**

**4.2 Bill of Materials** . . . . . **4-3**

## 4.1 Schematic

The schematic for the TPS54980EVM−022 is shown in Figure 4−1.

*Figure 4−1. TPS54980EVM-022 Schematic*



## 4.2 Bill of Materials

The bill of materials for the TPS54980EVM−022 is listed in Table 4−1.

*Table 4−1. TPS54980EVM-022 Bill of Materials*

| Count | Ref Des | Description | Size | MFR | Part Number |
|---|---|---|---|---|---|
| − | C1 | Capacitor, POSCAP, 220 µF, 10 V, 45 mΩ, 20% | 7343 (D) | Sanyo | 10TPB220M |
| 3 | C10, C14, C17 | Capacitor, ceramic, 0.1 µF, 25 V, X7R, 10% | 603 | Std | Std |
| 1 | C16 | Capacitor, ceramic, 1000 pF, 25 V, X7R, 10% | 603 | Std | Std |
| 7 | C2, C5, C9, C11, C12, C13, C19 | Capacitor, ceramic, 22 µF, 6.3 V, X5R, 20% | 1210 | Taiyo Yuden | JMK325BJ226MN |
| 1 | C3 | Capacitor, ceramic, 0.047 µF, 25 V, X7R, 10% | 603 | Std | Std |
| 1 | C4 | Capacitor, ceramic, 1.0 µF, 10 V, X5R, 20% | 603 | Std | Std |
| 2 | C6, C15 | Capacitor, ceramic, 3300 pF, 50 V, X7R, 10% | 603 | Std | Std |
| 1 | C7 | Capacitor, ceramic, 120 pF, 50 V, NPO, 5% | 603 | Std | Std |
| 1 | C8 | Capacitor, ceramic, 1200 pF, 50 V, X7R, 10% | 603 | Std | Std |
| 2 | J1, J3 | Terminal block, 2 pin, 15 A, 5,1 mm | 148830 | OST | ED1609 |
| 1 | J2 | Terminal block, 2 pin, 6 A, 3,5 mm | 75525 | OST | ED1514 |
| 1 | JP1 | Header, 2 pin, 100 mil spacing, (36-pin strip) | 0.100 × 2″ | Sullins | PTC36SAAN |
| 1 | JP2 | Header, 3 pin, 100 mil spacing, (36-pin strip) | 0.100 × 3″ | Sullins | PTC36SAAN |
| 2 | — | Shunt, 100 mil, black | 0.100 | 3M | 929950-00 |
| 1 | L1 | Inductor, 0.65 µH, 12 A | 0.340 × 0.250 | Pulse | PA0277 |
| 1 | R1 | Resistor, chip, 10.0 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | R10 | Resistor, chip, 0 Ω, 1/16 W, 1% | 603 | Std | Std |
| 1 | R11 | Resistor, chip, 2.4 Ω, 1/8 W, 1% | 1206 | Std | Std |
| 2 | R2, R7 | Resistor, chip, 9.76 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | R3 | Resistor, chip, 4.02 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | F4 | Resistor, chip, 71.5 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | R5 | Resistor, chip, 383 Ω, 1/16 W, 1% | 603 | Std | Std |
| 1 | R6 | Resistor, chip, 10.0 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | R8 | Resistor, chip, 6.04 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | R9 | Resistor, chip, 10 kΩ, 1/16 W, 1% | 603 | Std | Std |
| 1 | S1 | Switch, 1P2T, slide, PC mount, 200 mA | 0.46 × 0.16 | E_Switch | EQ1218 |
| 5 | TP1, TP3, TP4, TP5, TP6 | Test point, red, 1 mm | 0.038″, 6400″ | Farnell | 240-345 |
| 1 | TP10 | Test point, black, 1 mm | 0.038 | Farnell | 240-333 |
| 2 | TP2, TP8 | Test point, black, 1 mm | 0.038″, 6400″ | Farnell | 240-333 |

| Count | Ref Des | Description | Size | MFR | Part Number |
|---|---|---|---|---|---|
| 1 | TP7 | Adaptor, 3,5 mm probe clip (or 131-5031-00) | 72900 | Tektronix | 131-4244-00 |
| 1 | TP9 | Test point, red, 1 mm | 0.038 | Farnell | 240-345 |
| 1 | U1 | IC, high−side power distribution SW with current limit | SO8 | TI | TPS201xD |
| 1 | U2 | IC, tracking synchronous PWM switcher | PWP28 | TI | TPS54980PWP |
| 1 | — | PCB, 3 in. × 3 in. × 0.062 in. | | Any | HPA022 |

**Notes:** 1) These assemblies are ESD sensitive, ESD precautions should be observed.

2) These assemblies must be clean and free from flux and all contaminants, Use of no clean flux is not acceptable.

3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4) Reference designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent manufacturers components.